Introducing CXL™ 2.0 Specification
Industry Landscape

- Proliferation of Cloud Computing
- Growth of AI & Analytics
- Cloudification of the Network & Edge
CXL Delivers the Right Features & Architecture

**Challenges**
- Industry trends driving demand for faster data processing and next-gen data center performance
- Increasing demand for heterogeneous computing and server disaggregation
- Need for increased memory capacity and bandwidth
- Lack of open industry standard to address next-gen interconnect challenges

**CXL**
An open industry-supported cache-coherent interconnect for processors, memory expansion and accelerators

**Coherent Interface**
Leverages PCIe with 3 mix-and-match protocols

**Low Latency**
- Cache and Memory targeted at near CPU cache coherent latency

**Asymmetric Complexity**
Eases burdens of cache coherent interface designs
Representative CXL Usages

Caching Devices / Accelerators
- TYPE 1
  - Processor
  - DDR DDR
  - CXL
  - PROTOCOLS
    - CXL.io
    - CXL.cache
  - USAGES
    - PGAS NIC
    - NIC atomics

Accelerators with Memory
- TYPE 2
  - Processor
  - DDR DDR
  - CXL
  - PROTOCOLS
    - CXL.io
    - CXL.cache
    - CXL.memory
  - USAGES
    - GP GPU
    - Dense computation

Memory
- TYPE 3
  - Processor
  - DDR DDR
  - CXL
  - PROTOCOLS
    - CXL.io
    - CXL.memory
  - USAGES
    - Memory BW expansion
    - Memory capacity expansion
    - Storage class memory
Benefit of CXL 2.0 Switching
Expansion
Benefit of CXL 2.0 Switching

Memory/Accelerator Pooling with Single Logical Devices

CXL 2.0 Switch

Memory Pooling with Multiple Logical Devices

CXL 2.0 Switch

Standardized CXL Fabric Manager
Benefits of CXL 2.0 and Persistent Memory

- Moves Persistent Memory from Controller to CXL
- Enables Standardized Management of the Memory and Interface
- Supports a Wide Variety of Industry Form Factors

CXL + PM Fills the Gap!

<table>
<thead>
<tr>
<th>Memory</th>
<th>Latency (nanoseconds)</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU</td>
<td>$10^9$</td>
</tr>
<tr>
<td>DRAM CXL 1.1/1.0</td>
<td>$10^1$</td>
</tr>
<tr>
<td>CXL 2.0</td>
<td>$10^2 - 10^3$</td>
</tr>
<tr>
<td>Performance SSD</td>
<td>$10^4$</td>
</tr>
<tr>
<td>Capacity SSD</td>
<td>$10^5$</td>
</tr>
<tr>
<td>HDD</td>
<td>$10^6$</td>
</tr>
</tbody>
</table>

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CXL 2.0 Security Benefits

CXL 2.0 provides Integrity and Data Encryption of traffic across all entities (Root Complex, Switch, Device).
In Summary

CXL Consortium momentum continues to grow

- 150+ members and growing
- Celebrating first anniversary of incorporation – second generation specification
- Responding to industry needs and challenges

CXL 2.0 introduces new features & usage models

- Switching, pooling, persistent memory support, security
- Fully backward compatible with CXL 1.1 and 1.0
- Built in Compliance & Interop program

Call to action

- Join CXL Consortium
- Follow us on Twitter and LinkedIn for more updates!
Thank You